REMARKS

Claims 1-29 were pending in the application. Claims 4-5 have been cancelled. Claims 1, 2, 6, 7 and 9 have been amended. Claims 1, 2, 6, 7, 9, 10, 19 and 28 are independent claims. No new matter has been added.

Applicants respectfully submit that the present application is now in condition for allowance. Accordingly, reconsideration and allowance of the present application are respectfully requested.

Claim Amendments

Independent claim 1 has been amended. Support for the amendment is found, for example, at one or more portions of original claim 6.

Claims 2, 6, 7 and 9 have been amended to put these claims in independent form.

No new matter has been added.

Reconsideration and withdrawal of the rejections are respectfully requested.

Claim Rejections – 35 U.S.C. §102(b)

The Office Action rejects claims 1 and 4-5 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,004090 to Goto et al. ("Goto").

Reconsideration and withdrawal of the rejections are respectfully requested.

Claim 1

As stated above, independent claim 1 has been amended.

Independent claim 1 now recites a device comprising: a synchronization circuit to receive a synchronization signal, the synchronization signal substantially synchronized with a data transition, to synchronize the synchronization signal with a clock signal, and to generate a load signal based on the synchronized synchronization signal; and a ring counter to receive the load signal from the synchronization circuit and to circularly propagate the load signal; and a multiplexer to receive a plurality of delayed load signals from the ring counter, to receive an offset signal, and to output one of the plurality of delayed load signals based on the offset signal.

Goto et al. does not teach or suggest the device of independent claim 1.

Goto et al. disclose a bit synchronization circuit (title). A bit synchronization circuit shown in FIG. 2 is provided with a synchronization-controlling circuit 50, which receives a clock pulse from a clock pulse oscillator 11 and a pulse from a differential circuit 15 and supplies an output signal to the reset terminal of a first 4-scale ring counter 12 (col. 3, lines 44-49). The first 4-scale ring counter 12 counts clock pulses produced from the clock pulse oscillator 11 (col. 4, lines 5-6). An output from said ring counter 12 corresponding to the content 2 is applied to the reset terminal of a flip-flop circuit 13, and an output from said ring counter 12 corresponding to the content 0 is delivered to the set terminal of said flip-flop circuit 13 (col. 4, lines 6-11). The flip-flop circuit 13 generates an output signal synchronous with an input data signal received (col. 4, lines 11-13).

However, at the very least, Goto et al. does not teach or suggest a multiplexer to receive a plurality of delayed load signals from the ring counter, to receive an offset signal, and to output one of the plurality of delayed load signals based on the offset signal, as recited in claim 1.

Independent claim 1 should therefore be allowed.

Allowable Subject Matter

The Office Action states that claims 10-29 are allowed.

The Office Action objects to claims 2-3 and 6-9 as being dependent upon a rejected base claim, but states that such claims would be allowable if rewritten in independent form.

Claims 2, 6, 7 and 9 have been amended to put these claims in independent form.

Reconsideration and withdrawal of the objection to claims 2-3 and 6-9 are respectfully requested.

CONCLUSION

For at least the reasons set forth above, Applicants respectfully submit that the present application is in condition for allowance. Accordingly, reconsideration and allowance of the present application is respectfully requested.

Because the reasons set forth above are sufficient to overcome the rejections set forth in the outstanding Office Action, Applicants do not address some of the assertions set forth therein and/or other possible reasons for overcoming the rejections. Nonetheless, Applicants reserve the right to address such assertions and/or to present other possible reasons for overcoming the rejections in any future paper and/or proceeding.

If the Examiner believes that a telephone interview would expedite the prosecution of this application in any way, the Examiner is cordially requested to contact the undersigned via telephone at (203) 972-0006, ext. 1014.

Respectfully submitted,

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Date

Mark Steinberg
Registration No. 40,829
Buckley, Maschoff & Talwalkar LLC
Attorneys for Intel Corporation
50 Locust Avenue
New Canaan, CT 06840
(203) 972-0006, ext. 1014